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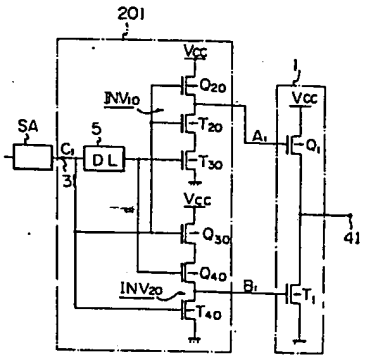
(54) A buffer circuit including inverter circuitry.

(57) A buffer circuit, for driving a C-MOS inverter, comprises a first and a second inverter for driving respectively a p-MOS transistor and an n-MOS transistor in the C-MOS inverter. Each of the inverters is connected in series with a switching transistor which is driven by a delay circuit so that, during a transition period of a C-MOS inverter, simultaneous conduction of current through the transistors of the inverter is prevented.

Fig. 3



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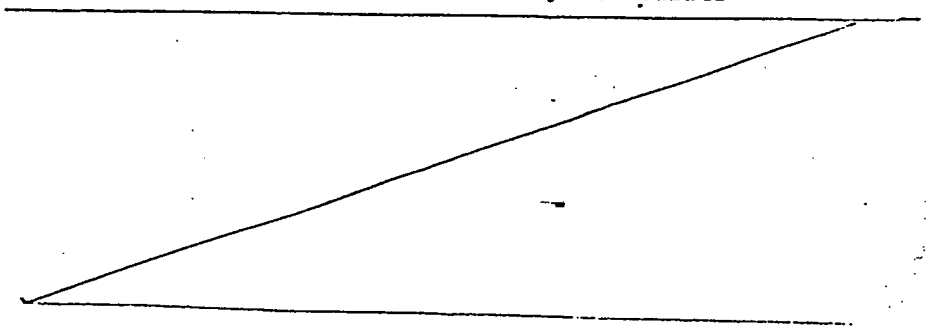
A BUFFER CIRCUIT INCLUDING INVERTER CIRCUITRY

The present invention relates to a buffer circuit including inverter circuitry, for example for driving a complementary metal-oxide semiconductor (C-MOS) inverter.

Generally, a conventional C-MOS inverter consists of a p-channel metal-oxide semiconductor (MOS) transistor (p-MOS) and an n-channel MOS transistor (n-MOS) connected in series between a power supply and a ground. In principle, no current flows from the power supply through the C-MOS inverter to the ground in a steady state. This is because when one of the p-MOS or n-MOS transistor is conductive (turned on), the other should be nonconductive (turned off). Therefore, there is no variation of the power supply voltage in the steady state.

During the transition period when the input of such a C-MOS inverter is inverted, however, there may be an instant when both transistors are conductive. At that instant, a large current flows through the C-MOS inverter. The large current causes a fluctuation in the power supply voltage which may be applied not only to the C-MOS inverter but also to an internal integrated circuit (IC) integrating the C-MOS inverter and to another external circuit. The momentary variation in the power supply voltage received by the internal IC or the external circuit as noise can cause error in circuit operation. Therefore, it is desirable to prevent such momentary large current during the above-mentioned transition period. This is especially true when the C-MOS inverter is used as an output circuit of, for example, a memory circuit.

A C-MOS inverter can be driven by two buffer



circuits for respectively driving the p-MOS transistor and n-MOS transistor in the C-MOS inverter. Conventionally, in order to prevent large currents during the above-mentioned transition period, the mutual conductances (gm) of the transistors which constitute the buffer circuits are made different from each other. This makes the timing for driving the p-MOS transistor different from the timing for driving the n-MOS transistor. However, it is somewhat difficult to manufacture the transistors in the buffer circuit to have exactly the right mutual conductances for obtaining the desired timing lag. Therefore, conventional buffer circuits may not prevent the momentary large current during the transition period of C-MOS inverters.

It is desirable to provide a buffer circuit, for driving a C-MOS inverter, which can prevent the simultaneous conduction of current through which constitute a C-MOS inverter, thereby to prevent fluctuations of the power supply voltage applied to the C-MOS inverter.

Desirably such a buffer circuit provided at the output stage of a semiconductor memory circuit, should prevent error operation of the semiconductor memory circuit due to fluctuations of the power supply voltage applied to the semiconductor memory circuit.

In an embodiment of the present invention there is provided a buffer circuit for driving a C-MOS inverter, the C-MOS inverter comprising a pair of transistors, the buffer circuit comprising a first inverter and a second inverter for inverting an input signal and for driving the pair of transistors in the C-MOS inverter, the first and second inverters each being connected between a power supply line and a ground, the first inverter having a first output

connected to one of the pair of transistors, and the second inverter having a second output connected to the other one of the pair of transistors, characterized in that, the first inverter comprises at least one first switching delay transistor inserted in series between the first output and the ground, the second inverter comprises at least one second switching delay transistor inserted in series between the power supply line and the second output, the first and second switching delay transistors operatively receive a delay signal with a predetermined delay time from the input signal, and the predetermined delay time is determined so as to prevent simultaneous conduction of current through the pair of transistors in the C-MOS inverter.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Fig. 1 is a circuit diagram illustrating a conventional buffer circuit for driving a C-MOS inverter;

Fig. 2 is a waveform diagram illustrating the relation between the input voltages and the output voltages of the buffer circuit in Fig. 1;

Fig. 3 is a circuit diagram illustrating a buffer circuit for driving a C-MOS inverter according to an embodiment of the present invention;

Fig. 4 is a waveform diagram illustrating the relation between the input voltages and the output voltages of the buffer circuit in Fig. 3;

Fig. 5 is a circuit diagram illustrating an example of a delay circuit for use in the circuit of Fig. 3;

Fig. 6 is a circuit diagram illustrating a buffer circuit for driving a C-MOS inverter according to another embodiment of the present invention; and

Fig. 7 is a circuit diagram illustrating a buffer circuit for driving a C-MOS inverter according to still

another embodiment of the present invention.

Before describing the embodiments of the present invention, a conventional example and its disadvantages will first be described with reference to Figs. 1 and 2. In Fig. 1, reference numeral 1 is a C-MOS inverter; 2 is a conventional buffer circuit for driving the C-MOS inverter 1; 3 is an input end of the buffer circuit 2; and 4 is an output end of the C-MOS inverter 1. Reference symbol SA represents a sense amplifier in a memory circuit. The C-MOS inverter 1 consists of a first p-MOS transistor Q_1 and a first n-MOS transistor T_1 connected in series between a power supply line V_{CC} and a ground. The buffer circuit 2 consists of a first inverter INV_1 for driving the first p-MOS transistor Q_1 and a second inverter INV_2 for driving the first n-MOS transistor T_1. The first inverter INV_1 consists of a second p-MOS transistor Q_2 and a second n-MOS transistor T_2 connected in series between the power supply line V_{CC} and the ground. The second inverter INV_2 consists of a third p-MOS transistor Q_3 and a third n-MOS transistor T_3 connected in series between the power supply line V_{CC} and the ground. The gates of the transistors in the buffer circuit 2 are commonly connected to the input end 3. The input end 3 is connected through the sense amplifier SA to a memory cell array (not shown). The connecting point between the p-MOS transistor Q_2 and the n-MOS transistor T_2, i.e., the output end of the first inverter INV_1, is connected to the gate of the first p-MOS transistor Q_1 in the C-MOS inverter 1. The connecting point between the p-MOS transistor Q_3 and the n-MOS transistor T_3, i.e., the output end of the second inverter INV_2, is connected to the gate of the first n-MOS transistor T_1 in the C-MOS inverter 1. The connecting point between the first p-MOS transistor Q_1 and the first n-MOS transistor T_1 is connected to the output end 4. In order to obtain a time lag between the output voltages A and B of the outputs of the first and second inverters INV_1 and INV_2, the mutual conductance gm of the

second n-MOS transistor T_2 is made smaller than that of the third n-MOS transistor T_3, or the mutual conductance gm of the second P-MOS transistor Q_2 is made greater than that of the third P-MOS transistor Q_3.

During the transition period when the input voltage C at the input end 3 falls from the power supply voltage (H level) to the ground voltage (L level), when the input voltage C becomes lower than the threshold voltages of the p-MOS transistors Q_2 and Q_3, the p-MOS transistors Q_2 and Q_3 are turned from their nonconductive states to their conductive states. When the input voltage becomes lower than the threshold voltages of the n-MOS transistors T_2 and T_3, the n-MOS transistors T_2 and T_3 are turned from their conductive states to their nonconductive states.

Since the mutual conductance gm of the p-MOS transistor Q_2 is made greater than that of the p-MOS transistor Q_3, the output voltage A rises earlier than the output voltage B, as illustrated in Fig. 2. The output voltages A and B are applied to the gates of the p-MOS transistor Q_1 and n-MOS transistor T_1 in the C-MOS inverter, respectively. The time lag of the output voltage B from the output voltage A during rising is τ_0.

If the time lag τ_0 could be made great, the p-MOS transistor Q_1 and n-MOS transistor T_1 in the C-MOS inverter 1 would not be simultaneously turned on. However, since the time lag τ_0 is usually too small, as illustrated in Fig. 2, there is an instant when both p-MOS transistor Q_1 and n-MOS transistor T_1 are turned on. That is, as shown in Fig. 2, t_1 is the time the output voltage B of the second inverter INV_2 reaches the threshold voltage V_{TH1} of the n-MOS transistor T_1 in the C-MOS inverter 1 and turns the n-MOS transistor T_1 from a nonconductive state to a conductive state. Now, t_2 is the time shortly after the time t_1 when the output voltage A of the first inverter INV_1 reaches the threshold voltage V_{TH2} of the p-MOS transistor Q_1 in the C-MOS inverter 1 and turns the p-MOS transistor Q_1 from a conductive state to a nonconductive state. Therefore, as

shown in Fig. 2, during the period between the times t_1 and t_2, both the p-MOS transistor Q_1 and the n-MOS transistor T_1 in the C-MOS inverter 1 are in their conductive states. As a result, a large current flows from the power supply line V_{CC} through the C-MOS inverter to the ground.

A substantially same discussion as described above applies to rising of the input voltage C. Accordingly, during the time t_3 and t_4, a large current also flows through the C-MOS inverter.

As mentioned before, a large current flowing through the C-MOS inverter, causes fluctuation of the power supply voltage V_{CC} and ground. This fluctuation of the power supply voltage can cause errors in internal or outer circuits connected to the same power supply line V_{CC} and ground. The problem is especially serious in circuits which require a plurality of C-MOS inverters, for example, in semiconductor memory circuits. In such circuits, the large currents flowing through the C-MOS inverters can accumulate to cause a considerable amount of voltage fluctuation in the power supply line.

Instead of designing the mutual conductance gm of the p-MOS transistor Q_2 to be greater than that of the p-MOS transistor Q_3, the mutual conductance gm of the n-MOS transistor T_2 may be made smaller than that of the n-MOS transistor T_3. This design also results in a time lag between the rising or falling waveforms of the output voltages A and B.

In any case, since it is considerably difficult to fabricate an MOS transistor so as to have just the right mutual conductance gm, the rising or falling waveforms of the output voltages of a conventional buffer circuit sometimes become close to each other, as illustrated in Fig. 2. Therefore, when a C-MOS inverter is driven by a conventional buffer circuit, the instantaneous large current can not surely be prevented from flowing through the C-MOS inverter during a transition period.

Embodiments of the present invention will now be described. In Fig. 3, a buffer circuit 201 for driving the C-MOS inverter 1 is illustrated. The C-MOS inverter 1 is the same as that in Fig. 1. The buffer circuit 201 of this embodiment comprises a first inverter INV_{10} for driving the first p-MOS transistor Q_1 and a second inverter INV_{20} for driving the first n-MOS transistor T_1. The first inverter INV_{10} comprises three transistors, i.e., a second p-MOS transistor Q_{20}, a second n-MOS transistor T_{20}, and a third n-MOS transistor T_{30} connected in series between the power supply line V_{CC} and the ground. The second inverter INV_{20} comprises three transistors, i.e., a third p-MOS transistor Q_{30}, a fourth p-MOS transistor Q_{40}, and a fourth n-MOS transistor T_{40} connected in series between the power supply line V_{CC} and the ground. A delay circuit 5 is provided between an input end 31 and the gates of the n-MOS transistor T_{30} and the p-MOS transistor Q_{40}. The gates of the p-MOS transistor Q_{20} and the n-MOS transistor T_{20} in the first inverter INV_{10}, and the gates of the p-MOS transistor Q_{30} and the n-MOS transistor T_{40} in the second inverter INV_{20}, are commonly connected to the input end 31. The gate of the n-MOS transistor T_{30} in the first inverter INV_{10} and the gate of the p-MOS transistor Q_{40} are commonly connected to the output of the delay circuit 5. The input end 31 may be connected through the sense amplifier SA to a memory circuit (not shown). The output of the first inverter INV_{10}, i.e., the connecting point between the p-MOS transistor Q_{20} and the n-MOS transistor T_{20}, is connected to the gate of the p-MOS transistor Q_1 in the C-MOS inverter 1. The output of the second inverter INV_{20}, i.e., the connecting point between the p-MOS transistor Q_{40} and the n-MOS transistor T_{40}, is connected to the gate of the n-MOS transistor T_1 in the C-MOS inverter 1. The output of the C-MOS inverter 1, i.e., the connecting point between the p-MOS transistor Q_1 and the n-MOS transistor T_1, is connected to an output terminal 41.

The main differences between the circuit of Fig. 1 and

the circuit of Fig. 3 are that, in Fig. 3, the first inverter INV_{10} includes the additional n-MOS transistor T_{30}; the second inverter INV_{20} includes the additional p-MOS transistor Q_{40} ; and the buffer circuit 30 includes the additional delay circuit 5. In this embodiment, it is not necessary to have different mutual conductances in the transistors in the buffer circuit 201, in order only to prevent an instantanous large current flowing through the inverter 1. Therefore, all the mutual conductances of Q_{20} , T_{20} , T_{30} , Q_{30} , Q_{40} and T_{40} can be determined only for the speed of driving the inverter.

The operation of the circuit of Fig. 3 is now described with reference to Fig. 4. During the transition period when the input voltage C_1 at the input end 31 falls from the H level to the L level, when the input voltage C_1 at the input end 31 reaches the threshold voltage V_{TH20} of the p-MOS transistors at a time t_5 , the p-MOS transistors Q_{20} and Q_{30} , the gates of which are directly connected to the input end 31, are turned from their nonconductive states to their conductive states. When the input voltage C_1 further decreases to reach the threshold voltage V_{TH10} of the n-MOS transistors, the n-MOS transistors T_{20} and T_{40} , the gates of which are directly connected to the input end 31, are turned from their conductive states to their nonconductive states. In the first inverter INV_{10} , after the input voltage C_1 becomes lower than the threshold voltage V_{TH10} , the p-MOS transistor Q_{20} is in the conductive state and the n-MOS transistor T_{20} is in the nonconductive state. Therefore, the output voltage A_1 of the first inerter INV_1 begins to rise. At a time t_6 , when the output voltage A_1 reaches the threshold voltage V_{TH20} of the p-MOS transistor Q_1 , the p-MOS transistor Q_1 is turned from on to off. On the other hand, in the second inverter INV_{20} , even at the time t_5 , the p-MOS transistor Q_{40} is not turned on because its gate receives the delayed input voltage from the delay circuit 5. Therefore, the output voltage B_1 begins to rise with a delay time after the rising of the output voltage A_1 of the

first inverter INV_{10}. At a time t_7 , when the output voltage B_1 reaches the threshold voltage V_{TH10} of the n-MOS transistor T_1 , the n-MOS transistor T_1 is turned from off to on. As a result, the output voltage at the output end of the C-MOS inverter 1 is turned from the H level to the L level. Before the time t_6 , only the p-MOS transistor Q_1 is in the conductive state. In the period between the time t_6 and t_7 , both p-MOS transistor Q_1 and n-MOS transistor T_1 are in the nonconductive state. After the time t_7 , only the n-MOS transistor T_1 is in the conductive state. Accordingly, during the transition when the input voltage C_1 falls, no momentary current flows from the power supply line V_{CC} through the p-MOS transistor Q_1 and n-MOS transistor T_1 to the ground.

During the rising of the input voltage C_1 , the n-MOS transistor T_{30} in the first inverter INV_{10} is turned on at the predetermined delay time τ after the n-MOS transistor T_{40} in the second inverter INV_{20} is turned on. Therefore, the output voltage A_1 of the first inverter INV_{10} falls with the delay time τ after the fall of the output voltage B_1 of the second inverter INV_{20}. The n-MOS transistor T_1 is turned off at a time t_8. After the time t_8 , the p-MOS transistor Q_1 is turned on at a time t_9. Before the time t_8 , only the n-MOS transistor T_1 is in the conductive state. Between the time t_8 and t_9 , both p-MOS transistor Q_1 and n-MOS transistor T_1 are in the nonconductive states. After the time t_9 , only the p-MOS transistor Q_1 is in the conductive state. Accordingly, no current flows through the C-MOS inverter 1 during the rising of the input voltage C_1.

Figure 5 shows an example of a well-known delay circuit adaptable to the delay circuit 5 in Fig. 3. The delay circuit of Fig. 5 comprises two inverters and a time constant circuit with a resistor R and a capacitor C. The resistance and the capacitance are appropriately determined so as to obtain the desired delay time τ.

The number of transistors in each inverter in the buffer circuit may alternatively be four or more so as to

realize three states, i.e., the L level, the H level, and a high impedance state, at the output of the C-MOS inverter 1. Figure 6 shows a buffer circuit for realizing the three states at the output of a memory circuit. The main difference between Fig. 3 and Fig. 6 is that, in Fig. 6, additional transistors Q_{22}, T_{32}, Q_{32}, and T_{42} are provided. The p-MOS transistor Q_{22} is connected in parallel to the p-MOS transistor Q_{20}. The n-MOS transistor T_{32} is inserted between the n-MOS transistor T_{30} and the ground. The p-MOS transistor Q_{32} is inserted between the power supply line V_{CC} and the p-MOS transistor Q_{30}. The n-MOS transistor T_{42} is connected in parallel to the n-MOS transistor T_{40}. The gates of the p-MOS transistor Q_{22} and the n-MOS transistor T_{32} are commonly connected to a terminal 6 which operatively receives a noninverted output enable signal. The gates of the p-MOS transistor Q_{32} and the N-MOS transistor T_{42} are commonly connected to another terminal 7 which operatively receives an inverted output enable signal.

In a standby state of the memory circuit, the output enable signal OE is at the L level, and the inverted output enable signal $\overline{OE}$ is at the H level. Therefore, the p-MOS transistor Q_{22} is on, and the n-MOS transistor T_{32} is off, so that the output voltage A_2 is at the H level regardless of the input voltage C_2. Accordingly, the p-MOS transistor Q_1 is off regardless of the input voltage C_2. Also, the p-MOS transistor Q_{32} is off and the n-MOS transistor T_{42} is on, so that the output voltage B_2 is at the L level regardless of the input voltage C_2. Consequently, the output of the inverter 1 is at a high impedance.

In an active state of the memory circuit, the output enable signal OE is at the H level, and the inverted output enable signal OE is at the L level. Therefore, the p-MOS transistor Q_{22} is off, and the n-MOS transistor T_{32} is on, so that the output voltage A_2 is at the H level or the L level depending on the L level or the H level of the input voltage C_1 respectively. Also, the p-MOS transistor Q_{32} is

on, and the N-MOS transistor T_{42} is off, so that the output voltage B_2 is at the H level or the L level depending on the L level or the H level of the input voltage C_2 respectively. The delay circuit 5 in Fig. 6 also gives a predetermined delay to the rising and the falling of the output voltages A_2 and B_2, in a similar way as in the circuit of Fig. 3.

In Fig. 7, still another embodiment of a buffer circuit is illustrated. In this embodiment, the buffer circuit 203 is composed of n-MOS transistors. No p-MOS transistor is used in this buffer circuit 203. In place of the p-MOS transistors Q_{20}, Q_{30}, and Q_{40} in Fig. 3, n-MOS transistors Q_{21}, Q_{31}, and Q_{41} are used in Fig. 7, respectively. Between the gate of the n-MOS transistor Q_{21} and the input end 33, a first inverter I_1 is inserted. Between the gate of the n-MOS transistor Q_{31} and the input end 33, a second inverter I_2 is inserted. Between the gate of the n-MOS transistor Q_{41} and the output of the delay circuit 5, a third inverter I_3 is inserted.

This construction enables a similar effect to be obtained as in the circuit of Fig. 3, as will be apparent to those skilled in the art.

The present invention is not restricted to the above-mentioned embodiments. Various other changes and modifications are possible without departing from the spirit of the invention. For example, the gates of the n-MOS transistors T_{20} and T_{30} may alternatively be connected to the output of the delay circuit 5 and to the input end 3, respectively. Also, the gates of the p-MOS transistors Q_{30} and Q_{40} may alternatively be connected to the output of the delay circuit 5 and to the input end 3, respectively. Further, the input signal of the buffer circuit may be supplied not only from a sense amplifier in a memory circuit but also from any other logic circuit.

From the foregoing description, it will be apparent that, in embodiments as described , since each of the two inverters for driving a p-MOS transistor and an n-MOS transistor in a C-MOS inverter consists of at least three

transistors and since delay circuit is inserted between an input end and the inverters, a desired delay time can be given to the driving timings of the transistors in the C-MOS inverter. As a result, simultaneous conduction of current through the transistors in the C-MOS inverter during its transition state can be prevented. Therefore, the voltage fluctuation of the power supply line, to which the C-MOS inverter and internal or outer circuits of the C-MOS inverter are connected, is suppressed. Further, power consumption in the C-MOS inverter can be reduced.

CLAIMS

1. A buffer circuit for driving a C-MOS inverter,

said C-MOS inverter comprising a pair of transistors,

said buffer circuit comprising a first inverter and a second inverter for inverting an input signal and for driving said pair of transistors in said C-MOS inverter,

said first and second inverters each being connected between a power supply line and a ground,

said first inverter having a first output connected to one of said pair of transistors, and

said second inverter having a second output connected to the other one of said pair of transistors,

characterized in that,

said first inverter comprises at least one first switching delay transistor inserted in series between said first output and said ground,

said second inverter comprises at least one second switching delay transistor inserted in series between said power supply line and said second output,

said first and second switching delay transistors operatively receive a delay signal with a predetermined delay time from said input signal, and

said predetermined delay time is determined so as to prevent simultaneous conduction of current through said pair of transistors in said C-MOS inverter.

2. A buffer circuit as set forth in claim 1, wherein said pair of transistors in said C-MOS inverter are a p-MOS transistor and and an n-MOS transistor; said first inverter comprises at least three transistors connected in series for driving said p-MOS transistor; said second inverter comprises at least three transistors connected in series for driving said n-MOS transistor; said buffer circuit further comprises a delay circuit for receiving said input signal and for providing said delay signal; at least one of said transistors in said first inverter being adapted to receive

said delay signal and at least one of said transistors in said second inverter being adapted to receive said delay signal.

3. A buffer circuit as set forth in claim 1 or 2, wherein said first inverter comprises a first p-MOS transistor connected to said power supply line and a first n-MOS transistor connected in series with said first p-MOS transistor, said first output being connected to a connecting point between said first p-MOS transistor and said first n-MOS transistor, said first switching delay transistor being a second n-MOS transistor connected between said first n-MOS transistor and said ground; and

said second inverter comprises a second p-MOS transistor connected to said power supply and a third n-MOS transistor connected to said ground, said second switching delay transistor being a third p-MOS transistor connected between said second p-MOS transistor and said third n-MOS transistor, said second output being connected to a connecting point between said third p-MOS transistor and said third n-MOS transistor.

4. A buffer circuit as set forth in claim 1 or 2, wherein said first inverter comprises a first p-MOS transistor connected to said power supply line and a first n-MOS transistor connected to said ground, said first switching delay transistor being a second n-MOS transistor connected between said first p-MOS transistor and said first n-MOS transistor, said first output being connected to a connecting point between said first p-MOS transistor and said second n-MOS transistor; and

said second inverter comprises a third n-MOS transistor connected to said ground and a second p-MOS transistor connected in series with said third n-MOS transistor, said second switching delay transistor being a third p-MOS transistor connected between said power supply line and said second p-MOS transistor, said second output being connected to a connecting point between said second p-MOS transistor and said third n-MOS transistor.

5. A buffer circuit as set forth in claim 1 or 2, wherein said first inverter comprises three n-MOS transistors, the first one of said n-MOS transistors being adapted to receive an inverted signal of said input signal, the second one of said n-MOS transistors being adapted to receive said input signal, and the third one of said n-MOS transistors being adapted to receive said delay signal; and said second inverter comprises three n-MOS transistors, the first one of said n-MOS transistors being adapted to receive an inverted input signal, the second one of said n-MOS transistors being adapted to receive an inverted signal of said delay signal, and the third one of said n-MOS transistors being adapted to receive said input signal.

6. A buffer circuit comprising first inverter circuitry connected between first and second power supply points and arranged to provide a first output signal of the buffer circuit, and second inverter circuitry connected between the said first and second power supply points and arranged to provide a second output signal of the buffer circuit, wherein each of the first and second output signals can have either a first value or a second value, the circuit being such as to operate on the basis of an input signal, applied to an input point of the circuit when it is in use, so that a change of the said input signal from one to the other of two predetermined working values thereof brings about respective changes of the said first and second output signals between the said first and second values thereof, reverse changes of those output signals being brought about by a reverse change of the said input signal, characterized in that a first switching device is connected in series with the first inverter circuitry between the said first and second power supply points, a second swithching device is connected in series with the second inverter circuitry between the said first and second power supply points, and delay circuitry is connected to apply to the first and second switching devices a control signal derived

from the said input signal but delayed so as to ensure that the first and second output signals will not be caused, by such a change of the said input signal, to have simultaneously a predetermined unwanted pair of respective values.

Fig. 1

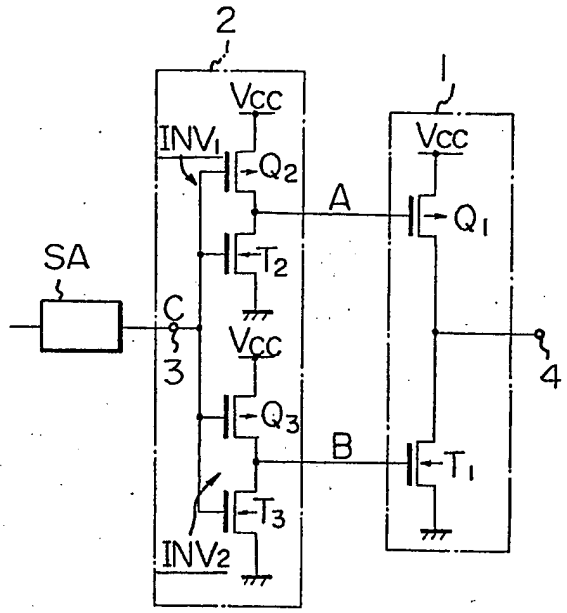

2
1
Vcc
Vcc
INV1
Q2
A
Q1
SA
T2
C
3
Vcc
4
Q3
B
T1
T3
INV2

Fig. 2

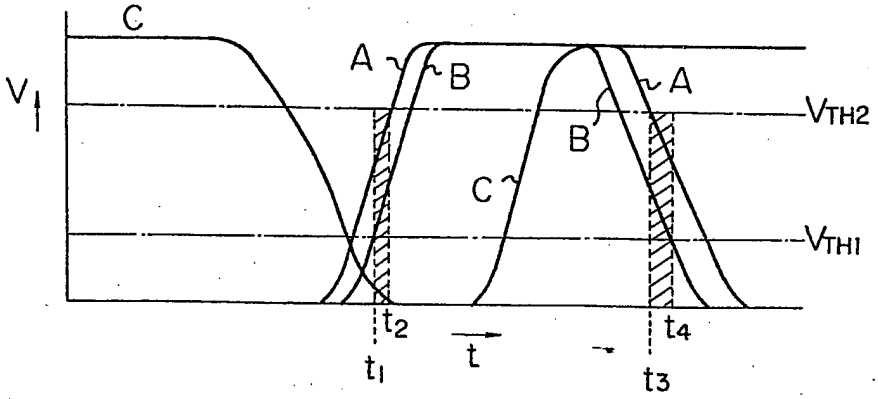
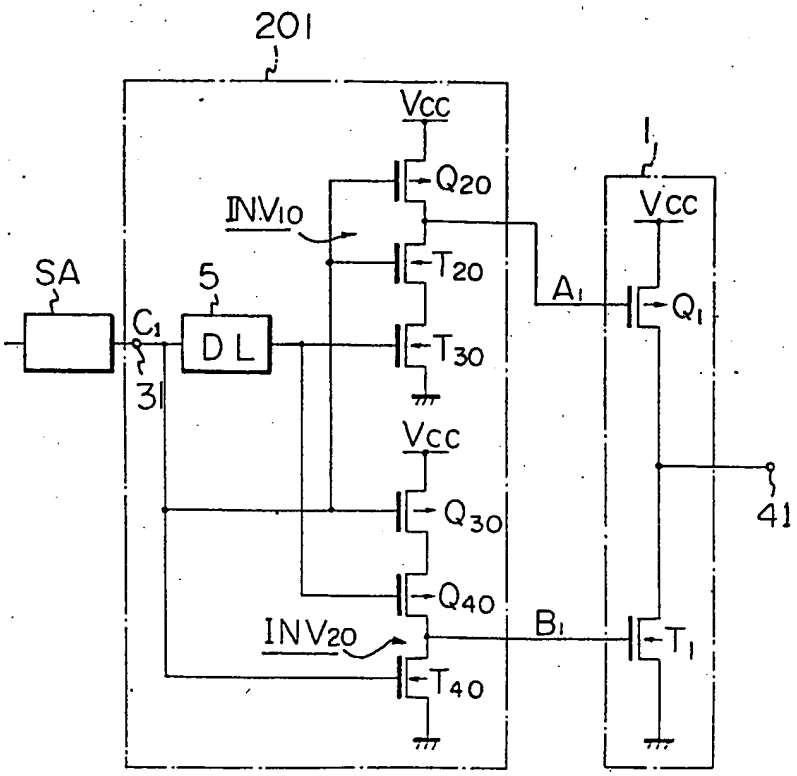

C
A
B
A
VTH2
B
C
VTH1
t2
t4
t1
t
t3

Fig. 3


201
Vcc
Q20
INV10
T20
SA
5
A1
Q1
C1
DL
T30
31
Vcc
Q30
41
Q40
B1
INV20
T1
T40

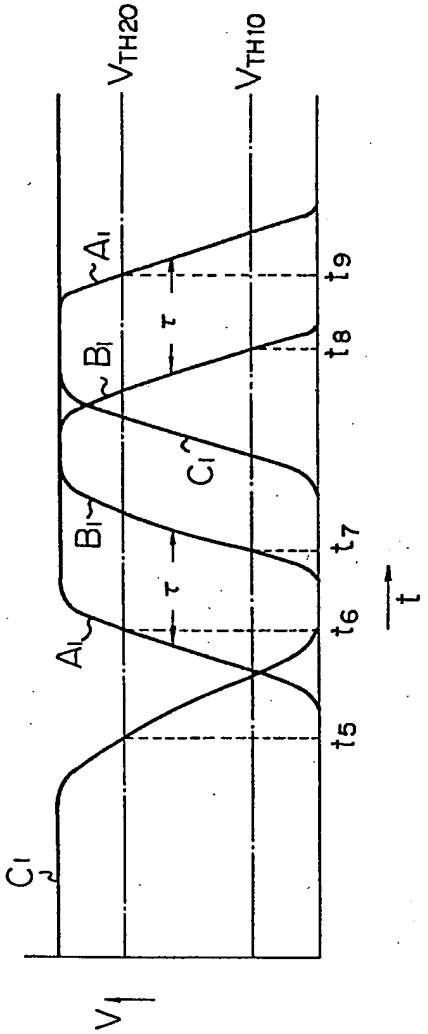


Fig. 4

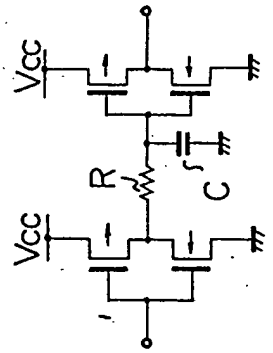


Fig. 5

Fig. 6

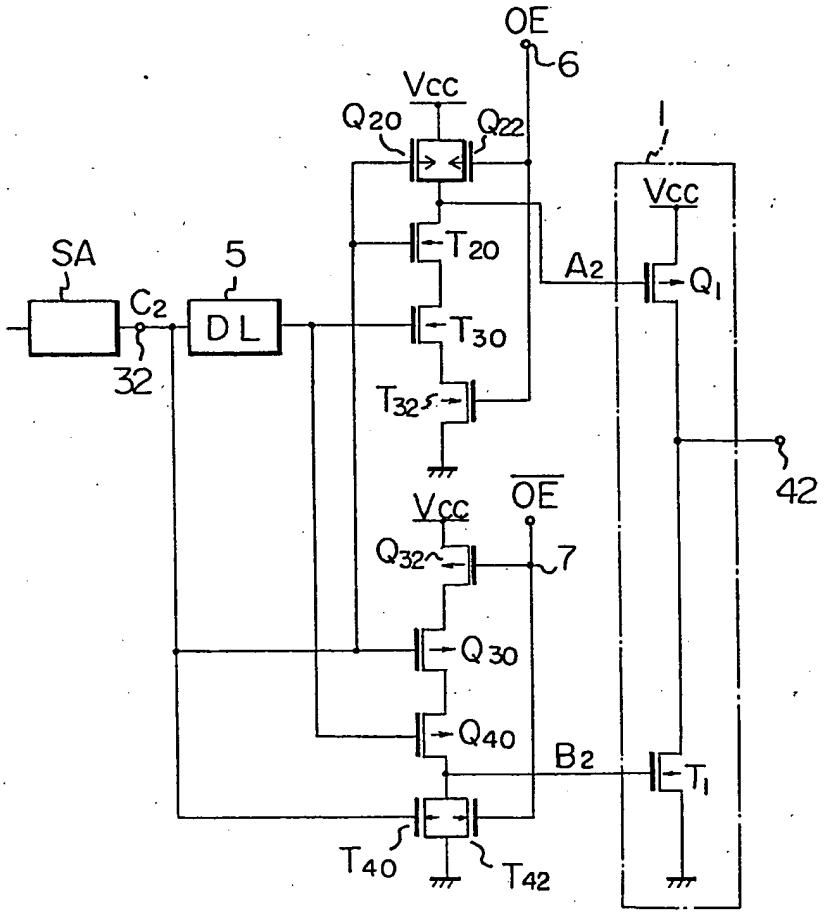
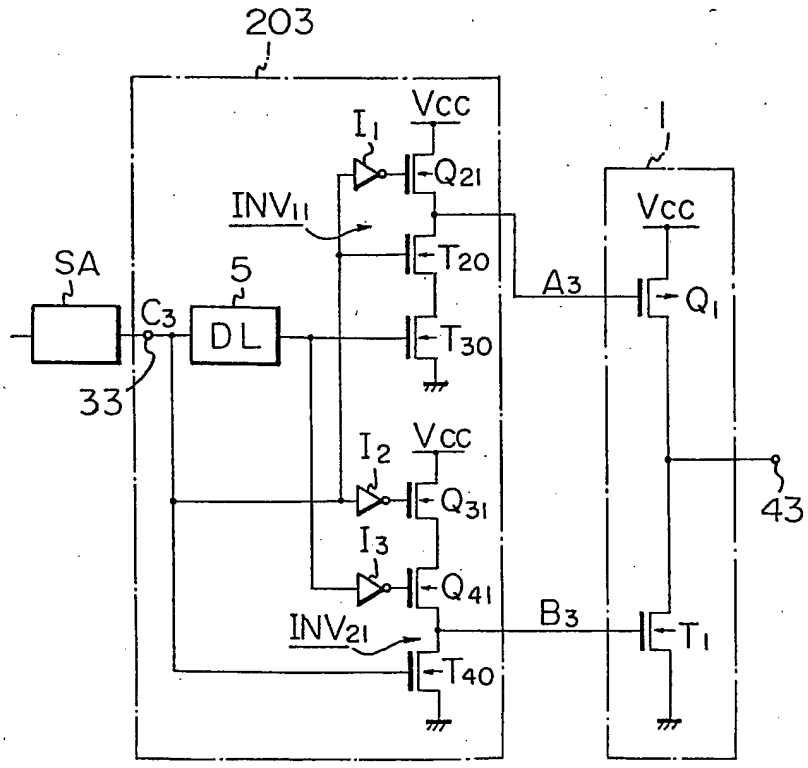

OE
6
Vcc
Q20
Q22
1
Vcc
SA
5
T20
A2
Q1
C2
DL
T30
32
T32
42
Vcc
OE
Q32
7
Q30
Q40
B2
T1
T40
T42

Fig. 7


203
Vcc
I1
Q21
INV11
T20
SA
5
A3
Q1
C3
DL
T30
33
I2
Vcc
Q31
43
I3
Q41
B3
INV21
T1
T40